The opinion is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHIH-HUANG CHANG AND SHAU-CHUO WEN,

Appeal 2007-2460
Application 10/709,179[1]
Technology Center 1700

Decided: 27 September 2007

Before FRED E. McKELVEY, *Senior Administrative Patent Judge*, and RICHARD E. SCHAFER and MICHAEL P. TIERNEY, *Administrative Patent Judges*.

TIERNEY, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a 35 U.S.C. § 134 appeal in the above-referenced case[2] of claims 15-20. Claims 1-14 have been cancelled. We have jurisdiction over the appeal pursuant to 35 U.S.C. § 6(b).

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[1] This application published as U.S. Published Application 2004/0207065 A1 on October 21, 2004.
[2] The real party in interest is Advanced Semiconductor Engineering, Inc. (Appeal Br. at 1).

STATEMENT OF THE CASE

Applicants' ("ASE's") invention relates to a method of fabricating bumps on the backside of a chip. (Specification, ¶ 3). ASE states that most electronic products are designed to be as light and compact as possible. (*Id.* at ¶ 6). To facilitate light and compact designs, multi-chip packages have been developed, such as having a plurality of chips stacked on top of each other and enclosed by a molding compound. (*Id.*). ASE's specification states that a method of fabricating bumps on the backside of a chip would have the potential to reduce the size of a multichip package structure. (*Id.* at ¶ 15).

There is one independent claim on appeal, claim 15. ASE states that claim 15 is representative of the claims on appeal for each of the rejections on appeal. (Appeal Br. at 4). Claim 15 is directed to a method of fabricating bumps on the backside of a chip. Specifically, claim 15 reads as follows:

> A method of fabricating bumps on a backside of a chip, comprising the steps of:
> providing the chip with an active surface having at least a bonding pad thereon and the backside;
> forming at least a bump pad on the backside of the chip; and
> forming a bump on the bump pad.

The Examiner made three (3) prior art rejections as follows:

i) Claims 15, 16 and 18 are rejected under 35 U.S.C. § 102(e) as anticipated by Ono, U.S. Published Application 2003/0107129 ("Ono")

> ii. Claims 17 and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ono as applied to claims 15-16 and further in view of Akram, U.S. Pat. 6,861,763 ("Akram")
>
> iii. Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Ono as applied to claims 15-16 and further in view of Koh, U.S. Published Application 2004/0135266

The application on appeal was filed on April 19, 2004 and claims foreign priority benefit of Taiwan application 92109018, filed April 18, 2003. Ono published on June 12, 2003, based upon an application filed August 27, 2001. Koh published on July 15, 2004 based upon an application filed March 1, 2004, which claims benefit of PCT/SG01/00058, filed April 6, 2001. Akram issued on March 1, 2005 based upon an application filed December 11, 2002. Ono, Koh and Akram are prior art under 35 U.S.C. § 102(e).[3]

ASE generally contends that a key aspect of its invention is the formation of bump pads on the back side of a chip. Specifically, ASE contends that:

> What significantly distinguishes the structure of this invention from the prior art references is that the present invention teaches providing a chip with a backside with at least a bump pad being formed on the backside of the chip and forming a bump on the bump pad on the backside of the chip.

(Appeal Br. at 6).

The Examiner found that Ono's semiconductor device has a bump on a bump pad that is located on the backside of a chip. In particular, the

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[3] ASE's Appeal Brief and Reply Brief do not attempt to antedate the prior art relied upon by the Examiner.

Examiner found that Ono teaches a chip, a first interconnector, a through hole, a second interconnector and a bump. Ono's first interconnector is attached to the backside of the chip, the through hole is located beneath the first interconnector and connects to a second interconnector, which is also beneath the first interconnector. Ono's bump attaches directly to the second interconnector. The Examiner found that a bump pad is understood by one of ordinary skill in the art to be a structure that provides an electrical connection between the bump and the semiconductor chip. The Examiner concluded that Ono teaches a bump on a bump pad that is on the backside of the chip as Ono's first and second interconnectors and through holes provide a structure that provides an electrical connection between Ono's bumps and Ono's semiconductor chip.

We affirm the Examiner's rejections.

ISSUE

The issue is whether Applicants have shown that the Examiner erred in rejecting the claims. Specifically, the issue is:

> Have Applicants demonstrated that the Examiner was unreasonable in construing a bond pad to be a structure that provides an electrical connection between a semiconductor chip and a bump?

FINDINGS OF FACT

A. ASE's '179 Specification and Claims

1) ASE's claims are directed to a method of fabricating bumps on a backside of a chip, comprising the steps of: [1] providing the chip with an active surface having at least a bonding pad thereon and the backside;

[2] forming at least a bump pad on the backside of the chip; and [3] forming a bump on the bump pad. (Appeal Br. Claims Appendix, Independent Claim 15).

2) ASE's specification states that its invention provides a method of fabricating bumps on the backside of a chip. ('179 Specification, ¶ 13).

3) ASE's specification teaches that a metallic layer is formed on the backside of a chip and the metallic layer is patterned to form a bump pad. (*Id.*).

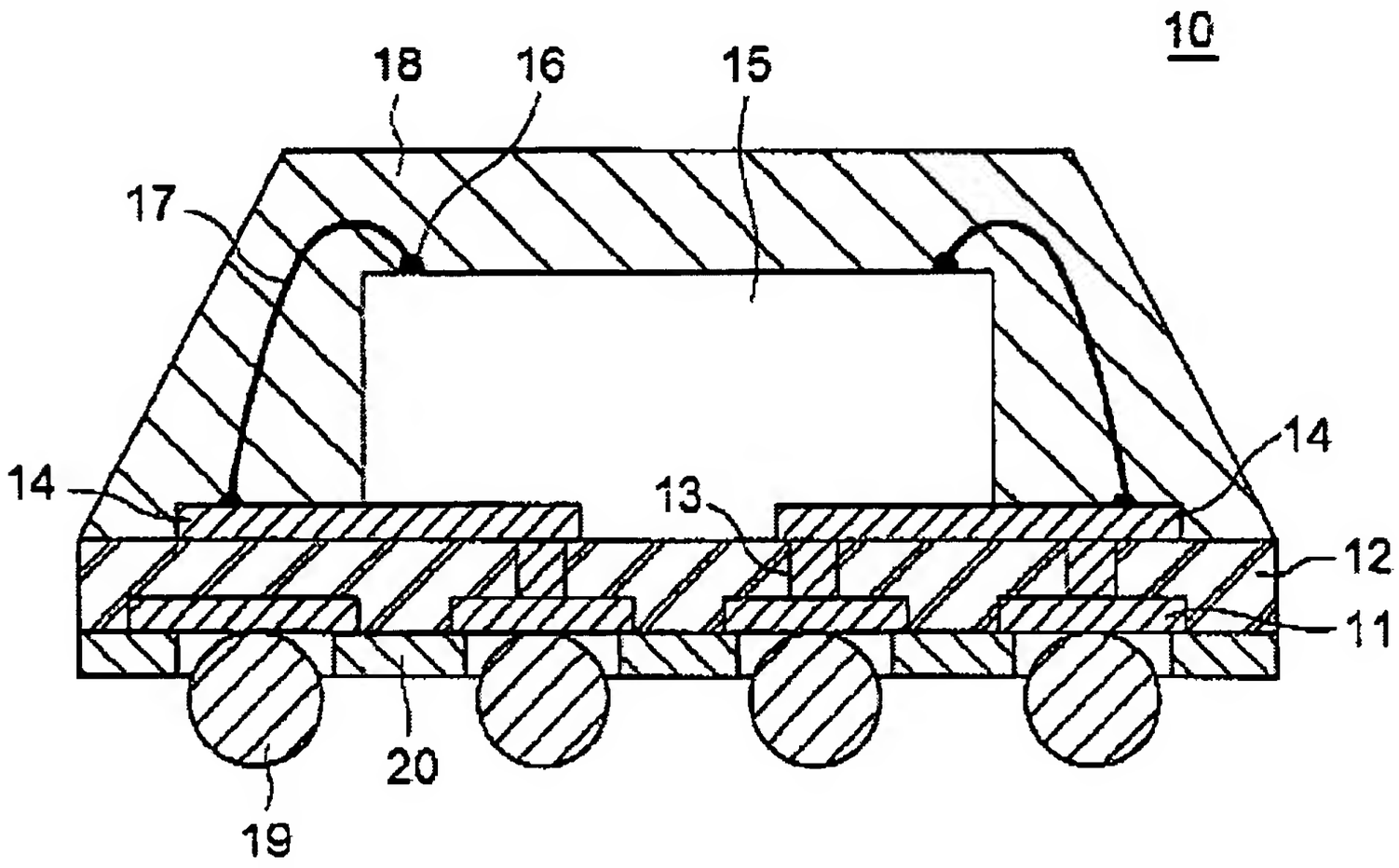
4) ASE's specification states that its bumps are attached to the metallic bump pads. (*Id.*).

B. The Prior Art

1. Ono, U.S. Pub. 2003/0107129

5) Ono is directed to method for fabricating a resin encapsulated semiconductor device. (Ono, Abstract).

6) Ono Figure 2, reproduced below, depicts a semiconductor device embodiment:



The semiconductor device depicted above includes:

11 First interconnect pattern
12 First dielectric layer
13 Through holes
14 Second interconnect pattern
15 Semiconductor chip
16 Electrodes
17 Bonding wires
18 Encapsulating resin
19 Metallic bumps
20 Adhesive dielectric sheet

(*Id.*, Fig. 2 and ¶ 28).

7) Ono provides the following explanation of what is depicted in Figure 2 of its published application:

> Referring to FIG. 2, a semiconductor device according to a first embodiment of the present invention has a first interconnect

> pattern 11, and a first dielectric layer 12 covering top and side surfaces of the first interconnect pattern 11. A second interconnect pattern 14 is formed on the first dielectric layer 12 and is connected to the first interconnect pattern 11 via through-holes 13 that are formed in the first dielectric layer 12 to penetrate the same. A semiconductor chip 15 is mounted on the first dielectric layer 12, and bonding wires 17 connect chip electrodes 16 formed on the semiconductor chip 15 with the second interconnect pattern 14. A encapsulating resin 18 encapsulates the semiconductor chip 15 and the bonding wires 17 on the first dielectric layer 12, and metallic bumps 19 constituting the external electrodes are formed on the bottom surface of the first interconnect pattern 11. An adhesive dielectric sheet 20 that constitutes a second dielectric layer covers the bottom surface of the first interconnect pattern 11 and exposes the bottom surface of the metallic bumps 19.

(*Id.* at ¶ 28).

8) Ono states that its Figure 3 is an example of a first interconnect pattern from a top view. (*Id.* at ¶ 29).

9) Ono states that the interconnect patterns may be formed from Ni, Cu and Au. (*Id.* at ¶ 56).

2. Akram, U.S. Pat. 6,861,763

10) Akram describes a method for forming packaged substrates. (Akram, Abstract).

11) Akram describes forming an array of bond pads at an active surface of a die, attaching conductive structures, such as conductive bumps to the

bonding pads and polymerizing a protecting layer in situ over the active surface. (Appeal Br. at 7 summarizing Akram).

3. Koh, U.S. Pub. 2004/0135266

12) Koh describes a substrate of non-electrically conducting material for mounting a semiconductor chip. (Koh, Abstract).

C. The Examiner's Answer

13) The Examiner found that Ono describes a method of fabricating bumps on a chip. (Answer, p. 3).

14) The Examiner found that one of ordinary skill in the art in the semiconductor packaging art would understand that a metal connection pad that electrically connects a bump to a chip is usually called a bump pad. (*Id.* at 6).

15) The Examiner found that Ono describes forming a bump pad structure on the backside of the chip as the first and second interconnect and through hole form a structure that electrically connects Ono's chip and metal bump. (*Id.*).

D. The Appeal Brief and Reply Brief.

16) ASE's Appeal Brief identifies claim 15 as representative of the claims on appeal as follows:

> For the first ground of rejection contested by appellant in this appeal, claims 15-16, 18 may be treated as one group, and independent claim 15 may be taken as the representative for the issue on appeal. For the second ground of rejection contested by appellant in this appeal, claims 15, 17 & 19 may be treated as one group to stand or fall together, and independent claim 15 may be taken as the representative for the issue on appeal. For the third ground of rejection contested by appellant in this appeal, claims 15 and 20, and claim 15 may be taken as the representative for issue on appeal.

(Appeal Br. at 4).

17) ASE's Reply Brief makes the following statement:

> However, to one of ordinary skills in the art, since the pattern 14 and bumps 19 are not even physically connected, the pattern 14 would not be considered bump pads but merely one of the interconnect types.

(Reply Br. at 8).

18) Both ASE's Appeal Brief and Reply Brief state that no evidence was submitted for review on appeal. (Appeal Br. at 12 and Reply Br. at 15).

PRINCIPLES OF LAW

During prosecution of a patent application, claims are given their broadest reasonable interpretation consistent with the specification. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969) (unpatented claims given broadest reasonable construction consistent with specification).

Anticipation under 35 U.S.C. § 102 is a question of fact. *Brown v. 3M*, 265 F.3d 1349, 1351, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001). A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. Inc. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

An invention is not patentable under 35 U.S.C. § 103 if it is obvious. *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1745-46, 82 USPQ2d 1385, 1400 (2007). The facts underlying an obviousness inquiry include:

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented.

Graham v. John Deere Co., 383 U.S. 1, 17-18 (1966). In addressing the findings of fact, "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR* at 1739, 82 USQP2d at 1395. As explained in *KSR*:

> If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* and *Anderson's-Black Rock* are illustrative — a court must ask whether the improvement is

> more than the predictable use of prior art elements according to their established functions.

KSR at 1740, 82 USPQ2d at 1396. As recognized in *KSR*, "[a] person of ordinary skill is also a person of ordinary creativity, not an automaton." *KSR* at 1742, 82 USPQ2d at 1397.

On appeal, Applicants bear the burden of showing that the Examiner has not established a legally sufficient basis for combining the teachings of the prior art. Applicants may sustain its burden by showing that where the Examiner relies on a combination of disclosures, the Examiner failed to provide sufficient evidence to show that one having ordinary skill in the art would have done what Applicants did. *United States v. Adams*, 383 U.S. 39 (1966).

ANALYSIS

There are three grounds of rejection on appeal, each of which is based upon prior art. The Examiner's rejections and ASE's response thereto are discussed below.

i) The Rejection of Claims 15, 16 and 18 under 35 U.S.C. § 102(e) as anticipated by Ono

ASE states that claim 15 is representative for the rejection of claims 15, 16 and 18. ASE claim 15 is a method of fabricating bumps on the backside of a chip. The claim requires that a bump pad be formed on the backside of the chip and that a bump be formed on the bump pad.

Scope of Claim 15

We provide claims with their broadest reasonable interpretation consistent with the specification. The Examiner states that bump pads are known in the art as structures that provide electrical connections between devices. This definition is consistent with ASE's specification, which identifies its bump pad as a metallic layer that connects a bump to the backside of a semiconductor chip. ('179 Specification, ¶ 13). We find no error in the Examiner's construction of the term "bump pad" as meaning structures that provide electrical connections between devices.

Applicability of Ono

ASE argues that one of ordinary skill in the art would not consider Ono's first and second interconnects and through holes to be a bump pad structure. Specifically, ASE states that Ono's bumps 19 and second interconnect 14 are not physically connected and thus the interconnect 14 would not be considered a bump pad. (Reply Br. at 8). ASE however, did not dispute that Ono's first and second interconnects and through holes define a structure that electrically connects Ono's bumps 19 to the backside of Ono's semiconductor chip 15. Further, ASE did not provide evidence to support its attorney argument as to how one ordinary skill in the art would interpret Ono's structure that electrically connects bumps to the backside of the chip. Based upon the record presented, we find that ASE has failed to establish that one of ordinary skill in the art would fail to understand that Ono's first and second interconnects and through holes form a

bump pad structure. *Rohm & Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092, 44 USPQ2d 1459, 1462 (Fed. Cir. 1997)(Nothing in the rules or in jurisprudence requires trier of fact to credit unsupported or conclusory assertions).

ASE contends that Ono does not teach forming a bump pad on the "backside" of a chip. (Appeal Br. at 6). ASE states that the Ono's second interconnect 14 is located on an area other than where the semiconductor chip 15 is located. (*Id.*). Ono Figure 2 however, clearly depicts the second interconnect 14 as being located on the backside of chip 15.

ASE argues that Ono Figure 2 is in error as the figure contradicts Figures 3-4B, especially Figure 3. (Reply Br. at 7). In particular, ASE states that none of the through holes 13 in Ono Figure 3 are aligned with or located right above the bumps 19, whereas Figure 2 depicts the through holes above or to the located right above of the bumps. (*Id.*).

Ono's second interconnect 14 of Figure 2 has a portion that is located beneath the chip 15 and a portion that extends beyond the semiconductor chip. The Examiner found that the through holes of Figure 3 represents an embodiment where the through holes are located underneath the portion of the second interconnect that extends beyond the chip. The Examiner's finding is consistent with Ono's figures and Ono's description of its figures. Furthermore, Ono states that Figure 3 is "an example" of the first interconnect in a top plan view and thus Ono's invention is not limited to what is depicted in Figure 3.

ASE argues that Ono describes its chip as located on an area other than where the semiconductor chip 15 is mounted. (Appeal Br. at 6 and Reply Br. at 8). The backside of Ono's chip 15 has a projection. The chip projection is identified as "mounted" on the first dielectric layer 12 and not the second interconnect 14. Yet, the non-projected portion on the backside of Ono chip 15 is placed on top of the second interconnect and ASE's claims do not require a bump pad extending across the entirety of the backside of the chip.

We AFFIRM the Examiner's rejection of claims 15, 16 and 18 over Ono.

ii. The Rejection of Claims 17 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Ono as applied to claims 15-16 and further in view of Akram

ASE identifies claim 15 as representative of claims 17 and 19. Yet, in addition to providing arguments with respect to claim 15, ASE comments that claim 17 differs from the teachings of Akram. ASE claim 17 depends from claim 15 and generally requires putting a mask on the backside of the chip, forming a metallic layer on the mask and removing the mask so that the remaining metallic layer on the backside of the chip becomes a bump pad.

ASE states that Akram describes the steps of forming a protective layer after bumps have been formed as opposed to before. ASE does not state that the differences between Akram and claim 17 are unobvious. (Appeal Br. at 7-8). Further, as noted by the Examiner, the selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. *In re Burhans*, 154 F.2d 690 (CCPA 1946); *In re*

Lang et al., 97 F.2d 626 (CCPA 1938) ("The fact that no single reference shows all the steps and that no reference shows the steps in the exact order named does not change the situation, since, in view of the prior art, what appellant has done would be the obvious thing to do in order to produce the claimed results.")

ASE states that the Examiner is incorrect in finding that Akram Figures 6-6A describe forming a protective layer on the backside of a chip. (Reply Br. at 10-11). Akram Figure 5 depicts a protective layer 34 that is applied to a backside of a chip at any convenient point in the semiconductor fabrication process and Akram Figure 6 depicts a protective layer 30 formed on the active surface of the chip. (Akram, Fig. 5-6A and col. 8, ll. 8-50). Thus, Akram describes placing a protective layer on both the active layer and the backside of the chip.

We AFFIRM the Examiner's rejection of claims 17 and 19 over Ono in view of Akram.

iii. The Rejection of Claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Ono as applied to claims 15-16 and further in view of Koh

ASE contends that claim 20 is allowable because the prior art fails to teach or suggest forming at least one bump pad on the backside of a chip. (Appeal Br. at 9). ASE states that claim 20 distinguishes over the prior art for the same reasons that claim 15 distinguishes over the prior art. (*Id.*).

For the reasons we affirm the Examiner's rejection of claim 15, we likewise AFFIRM the Examiner's rejection of claim 20 over Ono in view of Koh.

DECISION

ORDERED that the Examiner's rejection of claims 15, 16 and 18 under 35 U.S.C. § 102(e) as anticipated by Ono is *affirmed*.

FURTHER ORDERED that the Examiner's rejection of claims 17 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Ono as applied to claims 15-16 and further in view of Akram is *affirmed*.

FURTHER ORDERED that the Examiner's rejection of claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Ono as applied to claims 15-16 and further in view of Koh is *affirmed*.

AFFIRMED
(37 C.F.R. § 41.50(b) (2006)

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